AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1.   (Currently Amended) A software program stored on a computer-readable medium for monitoring and controlling a model railroad, said software program operable to perform the steps of:

displaying a representation of said model railroad layout on a display wherein a first portion of said model railroad layout is displayed using a first visual characteristic and a second portion of said model railroad layout is displayed using a second visual characteristic, wherein said first portion is selected to allow train movement thereon, and wherein said second portion is deselected to prevent train movement thereon; and

editing said representation of said model railroad layout, wherein editing comprises the steps of:

identifying a graphic type associated with a type of model railroad track to be edited; and

providing a list of editing functions based on the type of track to be edited, wherein said list includes a joining function if said track to be edited is a turnout section, a change length function if said track to be edited is a straight section and a trim function if said track to be edited is a curved section.

Claims 2-10 (Cancelled)

11.   (Previously Presented) An interface unit operable to translate a command received from a computer into a motor control command for controlling at least one element within a model railroad system, said interface comprising:

a plurality of addressable units for receiving address information and data information within said command, wherein one of said plurality of addressable units that corresponds to said address information within said command translates said data information into said motor control command and outputs said motor control command, wherein said plurality of addressable units includes a set of decoders and a plurality of addressable registers, and wherein said command includes three address bits, four group bits and one data bit.

12.   (Cancelled)

13.   (Previously Presented) The interface unit of claim 11, further comprising:
a resistor bank connected to each of said plurality of addressable registers.

14.   (Original) The interface unit of claim 13, further comprising:
a triac connected to each of said resistors in said resistor bank.

15.   (Previously Presented) The interface unit of claim 11, further comprising:
a coil latching relay connected to each of said plurality of addressable registers.

Claims 16-18 (Cancelled)

19.   (Previously Presented) The software program of claim 1, wherein said first visual characteristic is green; and
said second visual characteristic is red.

20.   (Previously Presented) A model railroad system comprising:

a graphical user interface displaying a representation of said model railroad system on a display, wherein a first portion of said model railroad layout is displayed using a first visual characteristic and a second portion of said model railroad layout is displayed using a second visual characteristic, wherein said first portion is selected to allow train movement thereon, and wherein said second portion is deselected to prevent train movement thereon;

said graphical user interface including an editing function that selectively permits a user to, rotate, move, delete and join a track portion based on a type of track portion which is selected; and

an interface unit controlled by said graphical user interface to translate a command received from a computer into a motor control command for controlling at least one element within a model railroad system, said interface unit including:

a plurality of addressable units for receiving address information and data information within said command, wherein one of said plurality of addressable units that corresponds to said address information within said command translates said data information into said motor control command and outputs said motor control command, wherein said plurality of addressable units includes a set of decoders and a plurality of addressable registers, and wherein said command includes three address bits, four group bits and one data bit.